What is claimed is:

1. A method of performing a numerical simulation, comprising:

programming a programmable device using a plurality of function blocks;

receiving input data;

providing a data path between a processor and the programmable device;

performing a first portion of the numerical simulation on the processor;

performing a second portion of the numerical simulation on the programmable device; and

exchanging data from at least one of the first and second portions via the data path.

2. The method of Claim 1, further comprising generating a plurality of function blocks.

3. The method of Claim 2, wherein generating a plurality of function blocks includes generating a plurality of VHDL function blocks.

4. The method of Claim 1, wherein exchanging data from at least one of the first and second portions via the data path includes providing inputs to a simulation block programmed into the programmable device from the processor via the data path.

5. The method of Claim 1, wherein exchanging data from at least one of the first and second portions via the data path includes providing outputs from a simulation block programmed into the programmable device to the processor via the data path.

6. The method of Claim 1, wherein performing a second portion of the numerical simulation on the programmable device includes performing a portion of the original simulation on the programmable device.

7. The method of Claim 6, wherein performing a portion of the simulation on the programmable device includes:

receiving inputs into a pair of gateway in blocks adapted to deliniate the portions of the simulation to convert into VHDL for operation in hardware.

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8. The method of Claim 7, wherein performing a portion of the simulation on the programmable device includes:

providing output from the programmable device.

9. The method of Claim 8, wherein performing a portion of a simulation on the programmable device includes:

coupling the outputs of the portion of the simulation to be run in hardware to at least one gateway out block adapted to deliniate the extent of the code to beconverted into VHDL for execution in hardware.

10. The method of Claim 1, wherein programming a programmable device includes programming a FPGA device.

11. The method of Claim 1, wherein receiving input data includes receiving first and second sine wave input data.

12. The method of Claim 1, further comprising:

forming a synthesis of the function blocks; and

synthesizing a file adapted for use to program gate connections of the programmable device.

13. A method of performing a numerical simulation, comprising:

generating a plurality of VHDL function blocks;

programming a programmable device using at least some of the plurality of function blocks;

receiving input data;

providing a data path between a processor and the programmable device;

performing a first portion of the numerical simulation on the processor;

performing a second portion of the numerical simulation on the programmable device; and

exchanging data from at least one of the first and second portions via the data path.

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14. The method of Claim 13, wherein exchanging data from at least one of the first and second portions via the data path includes providing inputs to a simulation block programmed into the programmable device from the processor via the data path.

15. The method of Claim 13, wherein exchanging data from at least one of the first and second portions via the data path includes providing outputs from a simulation block programmed into the programmable device to the processor via the data path.

16. The method of Claim 13, wherein programming a programmable device includes programming an FPGA device using at least some VHDL function blocks, and wherein performing a second portion of the numerical simulation on the programmable device includes performing an FFT on the programmable device.

17. The method of Claim 16, wherein performing a portion of a simulation on the programmable device includes:

receiving inputs via the data path into a pair of gateway in blocks;

coupling the output of the double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid;

coupling the output of a k=0 block to a fourth input of the FFT block, the fourth input being adapted to control a forward or a reverse transform;

providing a real component output from the FFT block;

providing an imaginary component output from the FFT block;

providing a third output from the FFT block adapted to mark the output data as valid or invalid;

providing a fourth output from the FFT block that is active high on a first output sample in a frame;

providing a fifth output from the FFT block that is active high when the FFT block can accept data;

coupling the real component output, imaginary component output, third output, fourth output, and fifth output from the FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and

coupling the outputs of the registers to at least one gateway out.

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18. The method of Claim 13, further comprising:

forming a synthesis of the function blocks; and

synthesizing a file adapted for use to program gate connections of the programmable device.

19. An apparatus for performing a numerical simulation, comprising:

an input device adapted to receive input data;

a processor adapted to perform a first portion of the numerical simulation;

a programmable device adapted to use at least some function blocks to perform a second portion of the numerical simulation; and

a data path coupled between the processor and the programmable device and adapted to exchange data from at least one of the first and second portions.

20. The apparatus of Claim 19, further comprising a generator adapted to generate a plurality of function blocks, at least some of the function blocks being adapted to perform a respective part of the second portion of the numerical simulation.

21. The apparatus of Claim 20, wherein the generator is further adapted to generate a plurality of VHDL function blocks.

22. The apparatus of Claim 19, wherein the programmable device includes an FPGA device.

23. The apparatus of Claim 19, wherein the input device is further adapted to receive input data.

24. The apparatus of Claim 19, the programmable device is further adapted to perform a simulation function block.

25. The apparatus of Claim 24, wherein the programmable device is further adapted to:

receive inputs into a pair of gateway in.

26. The apparatus of Claim 25, wherein the programmable device is further adapted to:

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provide output from the simulation block.

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